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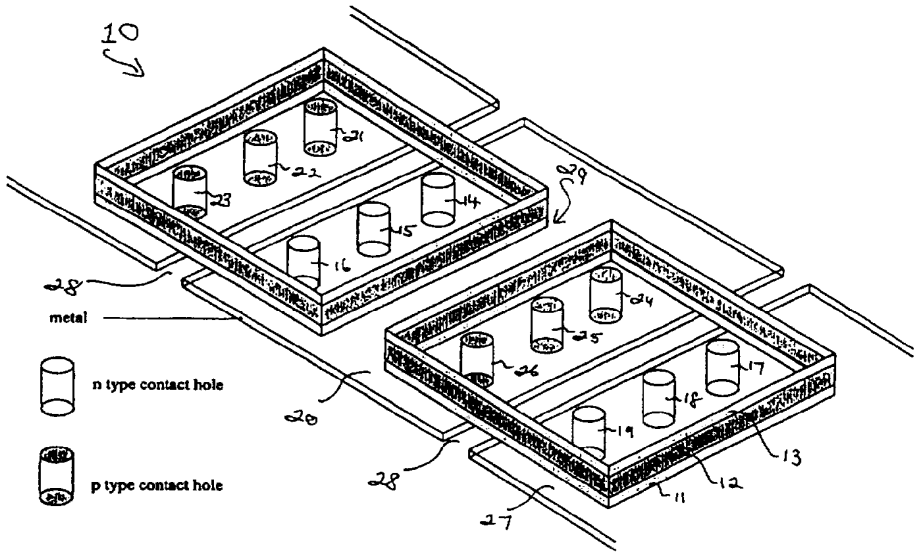

(57) Abstract

A contacting scheme for isolating and interconnecting the layers of a solar cell module (10) forms a plurality of series connected solar cells. N-type material layers (11, 13) are interconnected vertically by means of N-type pipes (14-19). The pipes then connect to a segment (20) of a conducting layer. P-type material layer (12) is conductively connected via P-type pipes (21-26) to another segment (27) of the conducting layer. Each segment (20, 27) is electrically isolated via separation (28). Individual groupings of PN junctions are isolated via a discontinuity (29) located through the layers of the thin film solar cell (10). The contacting scheme is suitable for use with both opaque and non-opaque substrates.

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Solar Cell Contacting Scheme

The present invention relates to a solar cell contacting scheme and, more particularly, to a method and means of interconnecting PN junctions on the one substrate. The invention is applicable, although not exclusively so, to thin film solar cell technology.

There is significant commercial impetus to provide more efficient and cheaper solar cells in a production environment. Figures of merit which are presently desirable include the achievement of a production cost of the order of a few Australian dollars per peak watt of solar cell modular capacity. Achievement of this figure would make solar cell technology extremely competitive compared with many other forms of power generation technology purely on economic grounds and without needing to take into account the inherently environmentally friendly nature of solar cell power generation schemes.

A particular area where efficiencies can be achieved is in the manner of interconnection of PN junctions on the one substrate. Presently a leading technology is generally termed the "buried contact" technology which involves interconnections being formed on a substrate by laying down electrical contact material continuously in a groove.

It is an object of the present invention to provide a solar cell contacting scheme which at least provides an alternative and, in some respects, may provide an improvement.

Brief Description of the Invention

Throughout this specification a means for conduction between and interconnection of semiconductor layers in a solar cell is referred to as a "pipe " or "pipes".

"Pipe is to be given a purposive construction. So, for example, the pipe can be of any cross-section in a plane of the semiconductor layers including by way of example circular, square, elongate oval, rectangular and the like.

As will be seen in some embodiments the pipes may be aligned along a longitudinal axis which is not perpendicular to the plane of the semiconductor layers and yet achieves the object and purpose of the invention.

Accordingly, in one broad from of the invention, there is provided in a solar cell module of the type comprising at least a first layer of a semiconductor of a first conductivity type and at least a second layer of a semiconductor of a second conductivity type, a method of insulating and interconnecting said layers so as to form a plurality of series connected solar cells.

Preferably said step of insulating said layers is performed by a discontinuity in said at least first layer and said at least second layer.

Preferably said step o interconnecting is performed by means of a segmented conducting layer.

Preferably said layer is in the form of a plane.

Preferably said step of interconnecting further includes providing at least a first conductive pipe of said first conductivity type and at least a second conductive pipe of said second conductivity type adapted to respectively connect said at least one layer of said first conductivity type to a segment of said segmented conducting plane and also connect said at least one layer of said second conductivity type to said segment of said segmented conducting plane so as to forma series connection between adjacent solar cells of said solar cell module.

Preferably said step of interconnecting further includes providing at least a first conductive groove of said first conductivity type and at least a second conductive groove of said second conductivity type adapted to respectively connect said at least one layer of said first conductivity type to a segment of said segmented conducting plane and also connect said at leat one layer of said second conductivity type to said segment of said segmented conducting plane so as to form a series connection between adjacent solar cells of said solar cell module.

Preferably said solar cell module comprises a plurality of stacked pairs of said at least first layer of a semiconductor of a first conductivity type.

Preferably said solar cell module is a thin film solar cell module.

Preferably said solar cell module is a silicon solar cell module.

Preferably said solar cell module is a polysilicon solar cell module.

Preferably said segmented conducting layer comprises a segmented metallic layer.

Preferably said segmented conducting layer is spaced from said at least first layer and said at least second layer by at least one electrically insulating layer.

Embodiments of the invention will now be described with reference to the accompanying drawings wherein:

Figures 1-8 illustrate steps in the preparation of a rear point contacting scheme according to a first embodiment of the invention;

Figures 9-13 illustrate steps in an alternative rear point contacting scheme for a metal substrate according to a second embodiment of the invention;

Figures 14-21 illustrate the steps in formation of a rear point contacting scheme for a glass superstrate according to a third embodiment of the invention;

Figures 22-26 illustrate an alternative rear point contacting scheme for a metal substrate according to a fourth embodiment of the invention;

Figures 27, 28 support a comparison of two versions of the present invention, one using isolated pipes and the other utilising continuous grooves for conduction to the segmented conducting layer;

Figure 29 is a generalised three dimensional, cut-away view of the solar cell contacting scheme suitable for use with any of the above described embodiments.

Figure 30 is a three dimensional, cut away view of the solar cell contacting scheme of Figure 8

Figure 31 illustrates methods of contacting pipe walls to to the conducting plane using a conductor (rather than a semi-conductor).

Detailed Description of Preferred Embodiments

With reference to Figure 29 there is shown a generalised three dimensional view of the contacting scheme of the invention applied to a thin film solar cell (10).

In this instance the solar cell comprises at least a first layer (11) of N-type material, a second layer (12) of P type material and a third layer (13) of N-type material.

The N-type material layers (11, 13) are interconnected vertically by means of N-type pipes (14, 14, 16, 17, 18, 19). These pipes then connect the layers vertically downwardly to a segment (20) of a segmented conducting layer, in this instance comprising a deposited metallisation.

Similarly the P-type material comprising second layer (12) is conductively connected via pipes (21, 22, 23, 24, 25, 26) to a second segment (27) of the segmented conducting layer. It will be noted that each segment (20, 27) is electrically isolated via separation (28).

Similarly individual groupings of PN junctions are isolated via a discontinuity (29) suitably located through the layers of the thin solar cell (10).

the end result is an interconnection system suitable for use with both opaque and non-opaque substrates as will be described in further detail with reference to particular embodiments to follow.

Figure 30 shows a corresponding layout based on the arrangement of Figure 8 (refer below).

The insulating layer between the segmented contacting layer and the semiconducting layers which is illustrated in subsequent specific embodiments to be described has been omitted from both Figures 29 and 30 for clarity. Such layer is necessary in the following embodiments to perform an insulating function.

Solar Cell Module Rear Point Contacting Scheme (#1a)

According to a first embodiment of the invention the steps in creation of the contacting scheme are described with reference to figures 1-8 as follows:

With reference to figure 1:

1. Deposit metal layer for conducting and reflecting (eg. Al), and scribe lines (laser or mechanical):

Note substrate could be conducting (eg. metal sheet), coated with an insulating di-electric layer. Alternatively, a glass *super*strate could be used with a transparent conducting oxide (TCO) instead of metal. This would result in a bi-facial cell (although with a less effective conductor & reflector).

With reference to figure 2:

2. Deposit di-electric layer(s) (for insulation, diffusion barrier, surface passivation and reflection).

3. For multi-junction cells, deposit n, p, n, p, n etc.

4. Laser ablation of contact holes through to metal, followed by p^+ silicon deposition (refer figure 3).

The varying depth of the hoes indicates the tolerance in manufacturing.

If the p^+ doping density required for a good contact is greater than that wanted in the device layer, then deposition should start initially with high doping and then reduce. It may be preferable for the thin highly doped layer to be outside the depletion region, in which case lower doped p type silicon should be deposited before the formation of the contact holes. This would also avoid the interruption of deposition which without ultra high vacuum may result in the formation of defects right at the most critical point (the metallurgical p-n junction).

5. Laser ablation of holes through to metal, followed by n^+ silicon deposition (refer figure 4).

Similarly, more lightly doped n type silicon than that required for the contacts may be deposited before the holes are formed. A thin, heavily doped silicon layer at the tip surface will be beneficial to voltage anyway. For floating emitter (top n layer), do step 5 before step 4 (n before p holes), then deposit final n layer.

Note if holes have a large diameter they may not be filled as shown, but rather lined. If hole diameter is comparable to the cell thickness, then forming holes at an angle will reduce or eliminate the "shading" loss (refer figure 5).

6. Scribe lines to produce individual cells and deposit passivating di-electric layer / AR coatings (refer figure 6).

⇒ layers connected in parallel, cells connected in series

Again, if line width is comparable to the cell thickness, then scribing lines at an angle will reduce or eliminate the "shading" loss.

In reality substrate and/or top surface are textured. A globular metal or TCO layer deposited in step 1 could perform this function.

The scheme is of course equally applicable for a single junction device.

7. Solid phase crystallisation of silicon layers (if necessary).

Cells of width 1mm, running the full length of the module and with a maximum power voltage of 0.5V, would develop 340V (=$\sqrt{2}$ x 240V) across a module of width 68cm. Wider cells would require contacts of both polarity over the full width of the cell (not just on one half as shown above) in order to avoid high series resistance losses within the silicon. If the metal layer is thick enough then the following simple design should have sufficiently low metal finger resistance (refer figure 7).

n and p are contact holes of the corresponding polarity, arrows show electron flow in metal.

Since metal covers the whole area, resistance along the fingers that run the full length of the module should not be great. A crude calculation would suggest that the metal layer would need to be only 9μm thick to carry the current along a 1m long module. (Buried contacts in wafer cells are spaced 1.2mm apart, have a cross sectional area of about 900μm^2 (25x35μm) and carry the current over 10cm. 1m would require 9000μm^2, which gives a thickness of 9μm for 1mm wide fingers). If metal layer is too thin (or TCO is uses) then a slightly more complicated contact scribe (step 1) would be necessary (eg. as described in contact scheme #2a for glass superstrates, refer figures 20 and 21).

A cross section of the module with wide cells would look like this (refer figure 8).

Contact holes of like polarity within each cell are connected together at the ends of the module as shown in figure 7.

Rear Point Contacting Scheme (#1b) for a Metal Substrate

A second embodiment of the invention will now be described with reference to figures 9-13 inclusive and comprises the following steps:

1. Deposit di-electric layer and rear n type silicon layer (refer figure 9).

2. For multi-junction, deposit p, n, p, n etc.

3. Laser ablation of holes through to metal, followed by p^+ silicon deposition (refer figure 10).

4. Laser ablation of holes through to metal, followed by n^+ silicon deposition (refer figure 11). Note that the hole is formed at an angle so that the shading loss is effectively zero.

5. Scribe individual cells and deposit passivation di-electric layer / AR coatings (refer figure 12).

6. Solid phase crystallisation of silicon layers (if Necessary).

7. Encapsulate, then scribe line in rear metal to isolate n from p contacts within individual cells (refer figure 13).

The metal line scribe requires accurate depth control. It could be done by covering the rear of the metal with any material that is not etched by a metal etchant, laser or mechanical scribing this material and then chemically etching the exposed metal.

Note that the encapsulate is the supporting layer once the continuity of the metal substrate is broken.

Rear Point Contacting Scheme (#2a) for a Glass Superstrate

A third embodiment of the invention will now be described with reference to figures 14-21 inclusive wherein the steps of manufacture of the contacting scheme are as follows:

1. Deposit silicon layers and crystallise (initial passivating di-electric layer / AR coating not shown) (refer figure 14).

2. Scribe individual cells and deposit di-electric (refer figure 15). (Note that for conventional cells, this step is reached simply by placing diffused, oxidised, un-contacted wafers on the glass).

3. Deposit metal (refer figure 16).

4. Laser ablation of contact holes, followed by n^+ silicon deposition (refer figure 17).

5. Laser ablation of p^+ contact holes, followed by p^+ silicon deposition (refer figure 18). Note p^+ silicon is connected to metal at the hole edges.

6. Scribe lines to isolate n^+ from p^+ within individual cells (refer figure 19).

The top n^+ and p^+ layers are not active layers in the solar cell and so do not have to be of good electronic quality; the quality of the junction between them is of no importance as they are shorted together by the metal layer anyway. The reason for their blanket coverage of the whole area is simply because this is technically easier than selective deposition on to the silicon contact areas that are exposed after hole formation.

For wide cells that require contacts of both polarity over the full width of the cell (not just on one half as shown in figure 19), but which have a metal layer too thin for the design described with reference to figure 19, a more complicated final isolation scribe would be necessary (refer figure 20). n and p are contact holes of the corresponding polarity. The same effect can be achieved using two sets of straight scribes (refer figure 21).

Alternative Rear Point Contacting Scheme(#2b) for a Metal Substrate

A fourth embodiment of the invention will now be described with reference to figures 22-26 inclusive and comprises the following steps:

1. Deposit de-electric layer and silicon layers (refer figure 22).
2. Scribe isolated cells, deposit de-electric and (if necessary) crystallise silicon (refer figure 23).
3. Laser ablation of contact holes, followed by n^+ silicon deposition (refer figure 24 which shows an inverted view relative to figure 23).
4. Laser ablation of holes, followed by p^+ silicon deposition (refer figure 25).
6. Attach to front encapsulant, then scribe lines to isolate n^+ from p^+ within individual cells (refer figure 26).

Note that the encapsulant is the supporting layer once the continuity of the metal substrate is broken.

The structure is now similar to scheme #2a for glass superstrates.

Comparison of different rear point contacting schemes

Schemes 2a & 2b

- 2 extra silicon deposition processes, but: -
- doping of the contacting layers can by chosen independently of the doping of the active layers.
- no high temperature processes whilst the silicon is in direct contact with the metal. (n^+ and p^+ contacting silicon layers can be deposited at low temperature). There is complete isolation over the whole area by the di-electric layer, whereas schemes 1a & 1b have the point contact

regions in contact with the metal during solid phase crystallisation, which may increase impurity diffusion into the active silicon layers.

- relative ease of patterning the silicon or metal in each scheme (see "scribing "below).

Possible advantages of metal substrate over glass superstrate

- metal deposition not necessary
- probably easier to texture a substrate such as metal sheet than silicon or glass (for light trapping and anti-reflection)
- growth on glass could produce very small grains at the interface, which is the top and most important part of the solar cell. This is quite likely if silicon is directly deposited as polycrystalline, or if crystallised on finely textured glass.
- solar cell could be flexible
- if encapsulated under glass, cheap, low temperature glass can be used
- substrate such as stainless steel would allow high temperature deposition

Comparison with Buried Contacts

Cell performance:

- Lower shading losses:

1. The required area of holes will likely be much less than for grooves; furthermore, since the holes are not metallised, light that does land on the holes can still be absorbed to produce collectable carriers. If the holes are large and only lined with either n or p silicon, then there will be no nearby collecting junction and so blue light will be lost, though red light can still be reflected from the rear reflector into the silicon layers at the side. Again, the blue light loss can be reduced by making the holes at an angle.
2. The lines through the metal contact layer will only reduce reflector performance; most reflection could occur at the silicon / di-electric interface anyway.
3. Since the isolation lines (for individual cells) scribed through the silicon do not carry current, they can be made as narrow as the laser beam can be focussed, so reducing "shading" losses. (possible eliminating them if lines are scribed at an angle). In any case, there is only one line per cell and even light that is incident on these lines can still be reflected sideways into the silicon.

- Since holes are likely to have lower shading losses, they could be closely spaced, thus lowering series resistance losses within the silicon. Series resistance in the wide metal fingers

will not be an issue, even perhaps if they spread the full length of a module.

- small area point metal contacts for minimum associated recombination losses and improved voltage
- Cell is not double sided (unless TCO used for scheme # 1a). How much of a disadvantage this is depends on the number of likely applications where modules can be mounted so as to receive a significant amount of light at the rear, as well as the extra cost of such mounting and the reduction in the light trapping performance of cells without a reflector.
- The success of the buried contact approach appears to rely on being able to sufficiently dope the walls of the groove *to the full depth* of the silicon *at the same time* as making the groove (otherwise the laser scribing time would be trebled and very precise alignment would be required to laser dope the existing groove walls). If such lasers are required to do this they may cause a large amount of damage to the surrounding silicon and substrate,. Even if a high temperature substrate is used, thus allowing conventional diffusion furnace doping, a masking layer would be required on the first set of grooves before doping the second set.
- My rear point contact scheme does not require laser assisted doping - this is all done by blanket CVD deposition, which is obviously not a problem. The only possible technical problem I can foresee for my scheme is the possible <u>diffusion of impurities from the metal layer into the silicon</u> during silicon deposition or crystallisation. For this reason, a metal other than aluminium may be used. Diffusion should not be a problem for scheme #2a for glass superstrates, since the only high temperature process required after metal deposition is the deposition of the *non-active* highly doped silicon layers for contacting. This can readily be done at < 500°C to produce micro-crystalline silicon. For substrates, diffusion during silicon growth and crystallisation can be minimised with a silicon nitride barrier, (most effectively in scheme #2b), which is easily deposited by CVD and will be necessary anyway for surface passivation and anti-reflection.
- All "thin" film crystalline silicon technologies could have problems with the adhesion of relatively thick (>1μm) layers to the sub/superstrate.

<u>Ease and Cost of Manufacturing</u>:

- buried contact method requires electroless plating of the grooves whilst the rear point contact schemes #1a & #2a require blanket metal deposition. Note that contact is made between the metal and the silicon only after making holes in the metal. This means a good ohmic contact is not required at the metal surface during deposition and therefore a number of non-vacuum,

low cost blanket metal deposition techniques could be used, possibly even simply bonding a metal foil to the substrate. It is possible that even with laser grooves a metal reflector would be required anyway, though this is only one reflector option.

- Rear point contact schemes #2a & #2b require 2 extra silicon deposition processes. These silicon layers do not have to be of good electronic quality and so can perhaps be deposited faster than other layers. There are no extra silicon deposition processes for schemes #1a & 1b, although the deposition of the final 2 layers is interrupted for the hole forming steps.
- The di-electric layers at the front and rear of the cell are necessary for both the buried contact and point contact methods.

Scribing:

- rear point contact scheme has lower alignment requirements - with buried contacts, the n grooves must be precisely aligned to the p grooves for series connection.
- Laser grooving and doping must be done in a vacuum chamber with a doping gas atmosphere. No chamber is necessary for the rear point contact scheme, though possibly helpful for sucking out debris.
- Some of the line scribes in the rear point contact scheme could be done mechanically. In scheme #1a, the metal lines could be made with cutting wheels, like a can opener, (rather than with diamond tipped grinders which probably wear down faster) or could even be stamped out or screen printed. The lines cut through the metal could be several hundred microns wide, with little effect on device performance. The required depth control in the other schemes may make mechanical patterning difficult.
- Mechanical forming of holes in silicon has also been demonstrated (by Willeke, Germany).
- For the rear point contact scheme, the holes (and lines) in the silicon can certainly be made with a u.v. laser, which will cause less damage to the surrounding silicon and substrate than with an i.r. laser. Simultaneous laser grooving and doping has not yet been demonstrated with a u.v. laser. A u.v. laser repeatedly ablates silicon to sub-micron depths with high pulse frequency, giving accurate depth control.

Scribing time:

- The rear point contact scheme appears to have more scribing than for buried contacts; however, the total length of the metal plus silicon line scribes is only equivalent to that for n plus p grooves.
- The holes are an extra step for the rear point contact scheme, but if grooves are formed by a

series of joined holes, as with present buried contact cells, then clearly it will be much faster to form widely spaced holes. On the other hand, if the grooves can be formed with a line focussed beam then they could be made as fast as holes.

- For modules with high output voltages (ie. many series connections),m the total scribe length for buried contacts would significantly increase, since series connection requires 2 grooves to be made next to each other.
- Parallelled mechanical scribing could be much faster and cheaper than laser scribing and is only possible for the rear point contact schemes.

In terms of comparison with groove systems for interconnection, it can be argued that the "pipe" system previously described is superior for the following reasons:

(a). Alignment tolerance (refer figure 27)

If the p^+ and n^+ silicon contacts were made via grooves as shown, rather than holes a previously described, then the regions shown in each unit cell would be wasted, since for the case of the right hand side, holes in the p layers will not be able to reach the p^+ contact, and likewise for the lower two n type layers on the left. These wasted regions can be reduced by moving the grooves to the edge of the isolation scribe, but this is at the expense of the same high alignment requirements as for the buried contact scheme.

(b). Scribing Time

Comparing the rear point contact scheme and the buried contact scheme, both have an extra line scribe for every unit cell. (A cell isolation scribe for the former scheme, and an extra scribe for adjacent n and p grooves in the latter). Consider the hole pattern of the former scheme to be made of lines consisting of a series of holes, as shown in (c) below. If the lines of n and p holes are equated to the n and p grooves of the buried contact scheme, then the metal scribe for the rear point contact scheme results I 50% more scribing than for buried contacts. However, since grooves are formed by a series of overlapping holes, the holes in the layout above could be made at least twice as fast as grooves, resulting in approximately equal total scribing times for both schemes.

The use of mechanical scribing, or a masked large area u.v. laser could significantly cut scribing times. These options are not available to the laser-doping buried contact scheme.

(c) Shading and resistive losses

It should be noted that the latest high efficiency PERL cells have point contacts on top and rear with out incurring series resistance problems. Also, for example, 20μm wide holes in a square

grid, evenly spaced in both directions by 124μm, would present the same shading loss as 20μm wide grooves spaced 1000μm apart. However, to prove the shading/series resistance advantage of holes, consider the layout below, where the spacing between the holes within a line equals the hole diameter. In this case, the total cross sectional contact area (ie. the total perimeter of the holes) will be the same as for grooves. The current flow lines will be almost identical and therefor, for the same line spacing, the series resistance within the active silicon layers will be the same as for buried contacts. However, the surface area and shading loss of holes will be halved (refer figure 28 which shows a plan view of the pipes of figure 6).

The other source of series resistance in the rear point contact scheme is in the current flow along the p^+ and n^+ silicon conductive pips/ holes, from the front to rear of the cell. For schemes 1(a) and 1(b), the thickness of these pipe walls equals that of the final active layer (ie. the emitter for n type material) and for the above hole layout the cross sectional area increasing the line spacing by the thickness of the device (this is the worst case for a single junction device). Thin film devices are likely to be only 5-10μm thick, whilst contact spacing is typically 500-1000μm, so the additional series resistance will only be about 1% of that in the active layers.

For schemes 2(a) and 2(b) the walls of the conductive pipes are formed by separate silicon deposition processes and could be doped to a conductivity 10-100 times higher than in the active layers. Even with a thickness 10 times less than that of the active emitter (eg. 0.1μm instead of 1μm), the series resistance losses would be less than 1% of that in the active layers.

The optimum efficiency layout of holes would be more widely spaced within a line, with more closely spaced lines, resulting in lower shading losses and/or resistive losses. However, more closely spaced lines would increase the number of scribes and total scribing time. It would also degrade reflector performance, unless a transparent conducting oxide was used in place of the rear metal, along with a separate detached reflector. eg. 20μm wide lines spaced 200μm apart in the reflecting contact metal would represent a degraded are of 10%.

The buried contact scheme also has the disadvantage of requiring a certain minimum line width in order to fill the groove with sufficient metal to reduce finger resistance. For thin film cells 4-8 times thinner than the present groove depth in wafered devices, the groove width may need to be significantly increased beyond the 20μm used in these devices. In contrast, decreasing the hole width as far as technically possible, and reducing the spacing of holes, will continually increase the efficiency of the rear point contact scheme.

In conclusion, for equal scribing times and the same series resistance, the rear point contact scheme will have at least half the shading losses of the buried contact scheme. It will also have lower alignment requirements.

Claims

1. In a solar cell module of the type comprising at least a first layer of a semiconductor of a first conductivity type and at least a second layer of a semiconductor of a second conductivity type, a method of insulating and interconnecting said layers so as to form a plurality of series connected solar cells.
2. The method of claim 1 wherein said step of insulating said layers is performed by a discontinuity in said at least first layer and said at least second layer.
3. The method of claim 1 or 2 wherein said step of interconnecting is performed by means of a segmented conducting layer.
4. The method of claim 3 wherein said layer is in the form of a plane.
5. The method of claim 3 or 4 wherein said step of interconnecting further includes providing at least a first conductive pipe of said first conductivity type and at least a second conductive pipe of said second conductivity type adapted to respectively connect said at least one layer of said first conductivity type to a segment of said segmented conducting plane and also connect said at least one layer of said second conductivity type to said segment of said segmented conducting plane so as to form a series connection between adjacent solar cells of said solar cell module.
6. The method of claim 3 or 4 wherein said step of interconnecting further includes providing at least a first conductive groove of said first conductivity type and at least a second conductive groove of said second conductivity type adapted to respectively connect said at least one layer of said first conductivity type to a segment of said segmented conducting plane and also connect said at least one layer of said second conductivity type to said segment of said segmented conducting plane so as to form a series connection between adjacent solar cells of said solar cell module.
7. The method of claim 5 or 6 wherein said solar cell module comprises of plurality of stacked pairs of said at least first layer of a semiconductor of a first conductivity type.
8. The method of claim 7 wherein said solar cell module is a thin film solar cell module.
9. The method of claim 8 wherein said solar cell module is a silicon solar cell module.
10. The method of claim 9 wherein said solar cell module is a polysilicon solar cell module.
11. The method of any previous claim wherein said segmented conducting layer comprises a segmented metallic layer.
12. The method of any previous claim wherein said segmented conducting layer is spaced from said at least first layer and said at least second layer by at least one electrically insulating layer.
13. A solar cell module made according to the method of any preceding claim.

14. A solar cell module as hereinbefore particularly described with reference to any one of figure 29, figure 30, figures 1-8, figures 9-13, figures 14-21 or figures 22-26 or Fig 31.

15 The method of any previous claim wherein said conductive pipes are adapted to connect to said conducting plane by means of a continuation in length of the said pipes of said first or second conductivity type as far as said conductive plane.

16 The method of any previous claim wherein said conductive pipes are adapted to connect to said conducting plane by means of any other semiconductor material, or metal, or transparent conductor, or any other conducting material forming a connection between said conductive pipes and said conducting plane.

17 The method of any previous claim wherin said segmented conducting layer is spaced from said at least first layer and said at least second layer by at least one layer of transparent conductor.

18 The method of any previous claim wherein fabrication proceeds by the following steps:
deposit the active layers
scribe into individual cells
deposit dielectric
scribe holes for p-type pipes
deposit heavily doped p-type silicon
optional - deposit TCO
scribe holes for n-type pipes
deposit heavily doped n-type silicon
(or do n-typr first, then p-type)
deposit TCO
deposit metal
1. scribe metal/TCO/heavily doped Si layers

19 The method of any previous claim wherein fabrication proceeds by the following steps:
deposit the active layers
scribe into individual cells
deposit dielectric
optional - deposit TCO
scribe holes for p-type pipes
deposit heavily doped p-type silicon
optional - deposit TCO
scribe holes for n-type pipes
deposit heavily doped n-type silicon
(or do n-typr first, then p-type)
deposit TCO
deposit metal
scribe metal/TCO/heavily doped Si layers

20 A solar cell made by the method of any one of claims 15 to 19.

1. deposit metal layer for conducting and reflecting (eg. Al), and scribe lines (laser or mechanical):

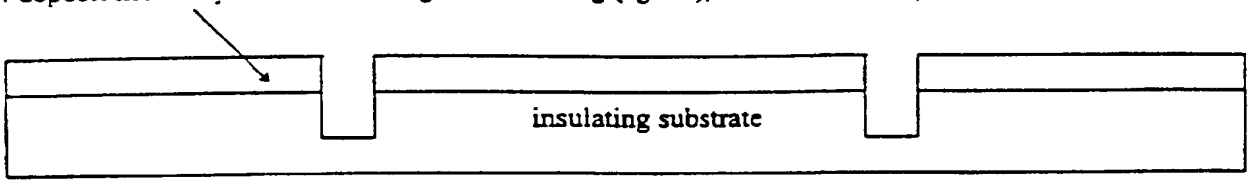


Fig 1

2. deposit di-electric layer(s) (for insulation, diffusion barrier, surface passivation and reflection):

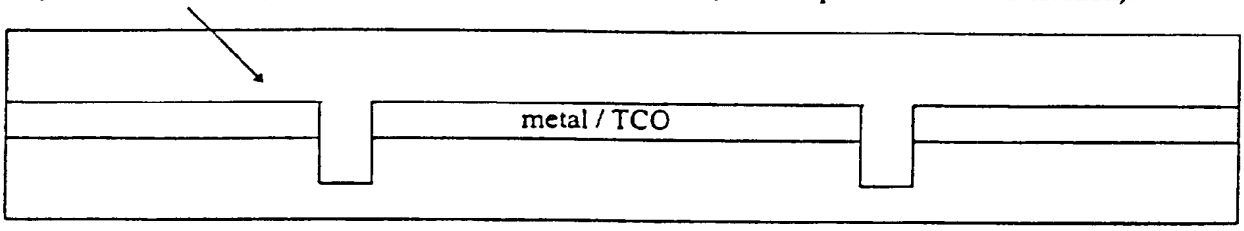
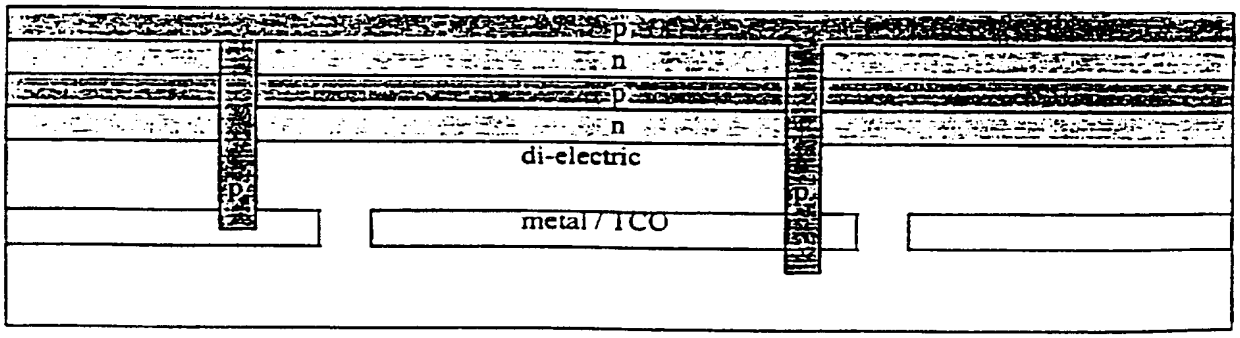


Fig 2

4. laser ablation of contact holes through to metal, followed by p^+ silicon deposition:



The varying depth of the holes indicates the tolerance in manufacturing.

Fig 3

5. laser ablation of holes through to metal, followed by n^+ silicon deposition:

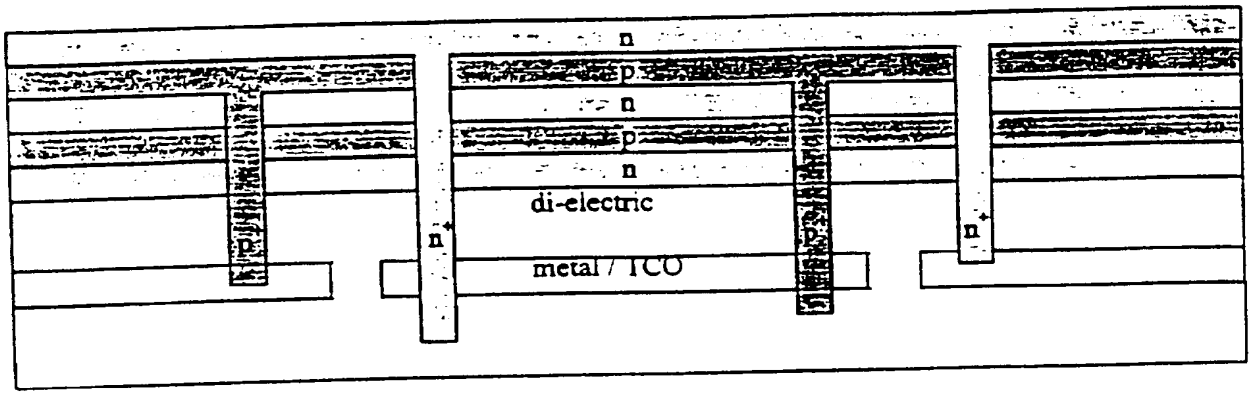


Fig 4

Note if holes have a large diameter they may not be filled as shown, but rather lined. If hole diameter is comparable to the cell thickness, then forming holes at an angle will reduce or eliminate the "shading" loss:

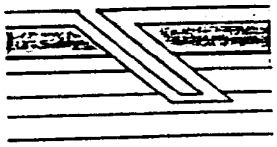
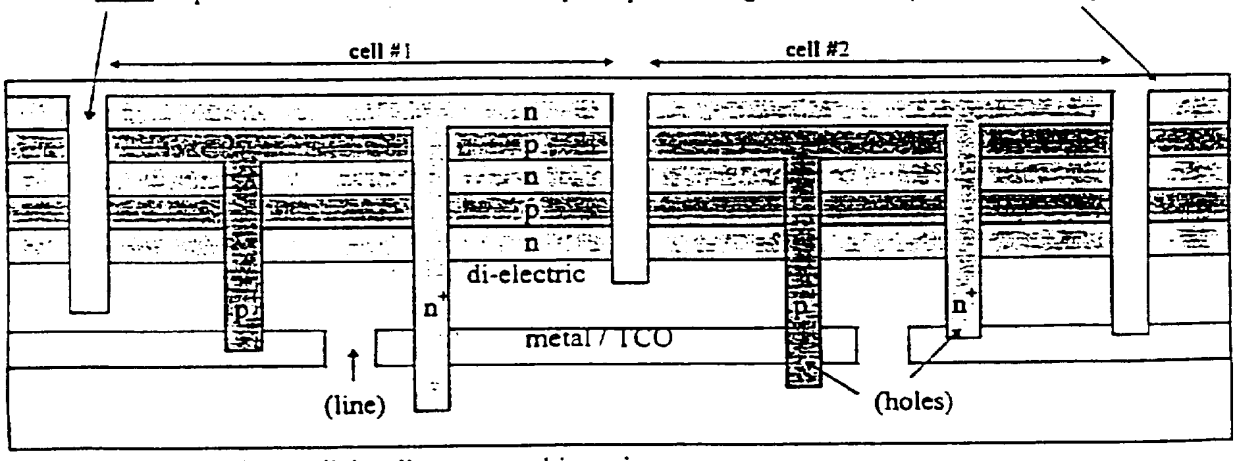


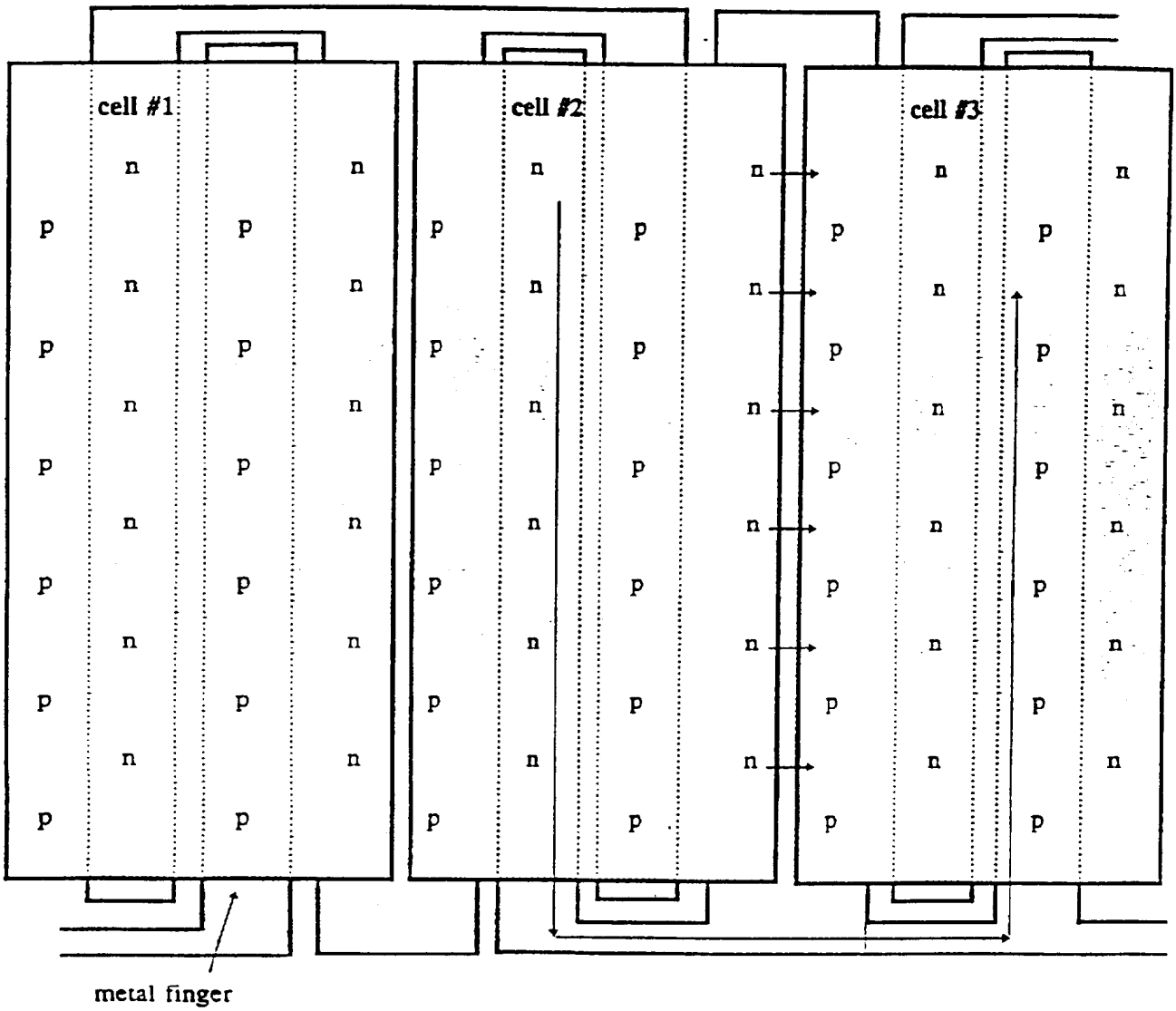
Fig 5

6. scribe lines to produce individual cells and deposit passivating di-electric layer / AR coatings:



⇒ layers connected in parallel, cells connected in series

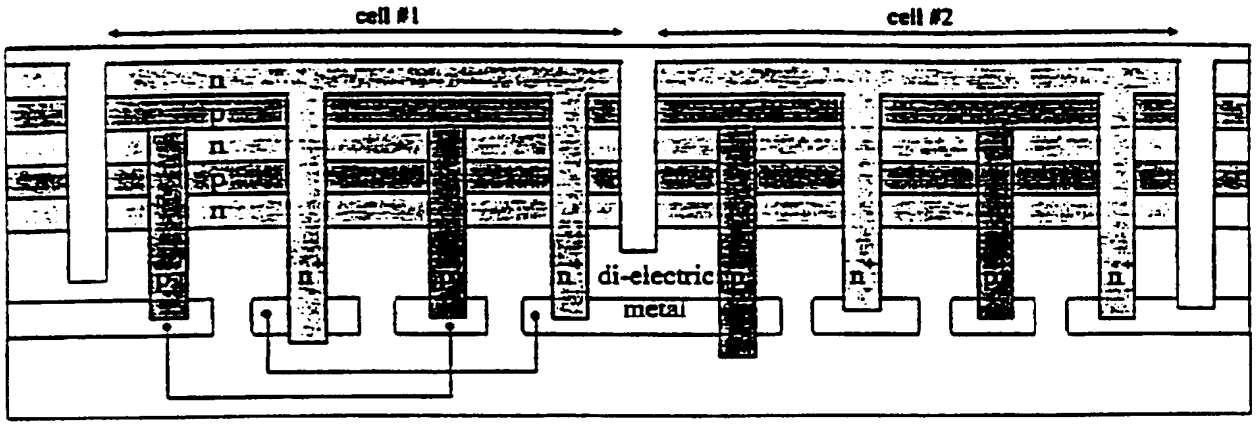
Fig 6



n and p are contact holes of the corresponding polarity, arrows show electron flow in metal.

Fig 7

A cross section of the module with wide cells would look like this:



Contact holes of like polarity within each cell are connected together at the ends of the module as shown in the previous diagram.

Fig 8

Rear Point Contacting Scheme (#1b) for a Metal Substrate

1. deposit di-electric layer and rear n type silicon layer:

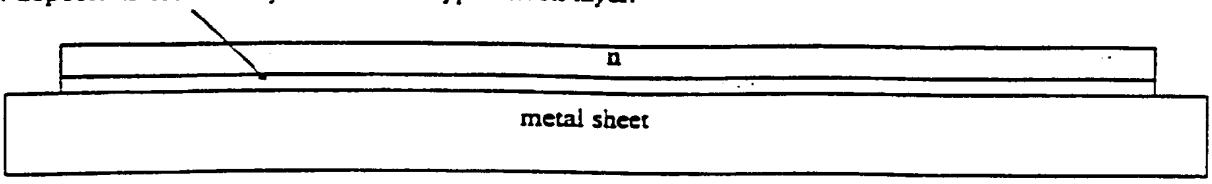


Fig 9

2. for multi-junction, deposit p,n,p,n etc.

3. laser ablation of holes through to metal, followed by p^+ silicon deposition:

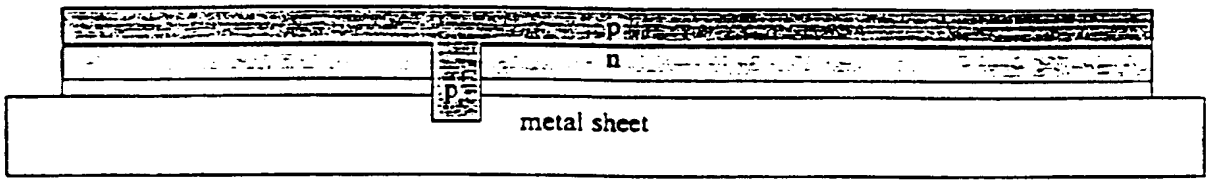
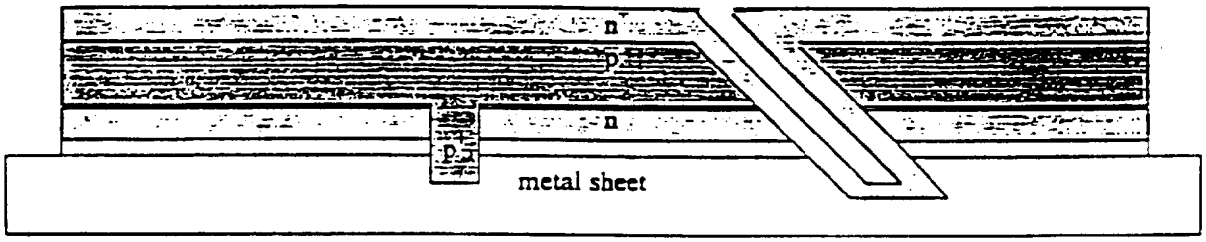


Fig 10

4. laser ablation of holes through to metal, followed by n^+ silicon deposition:



Note that the hole is formed at an angle so that the shading loss is effectively zero.

Fig 11

5. scribe individual cells and deposit passivating di-electric layer / AR coatings:

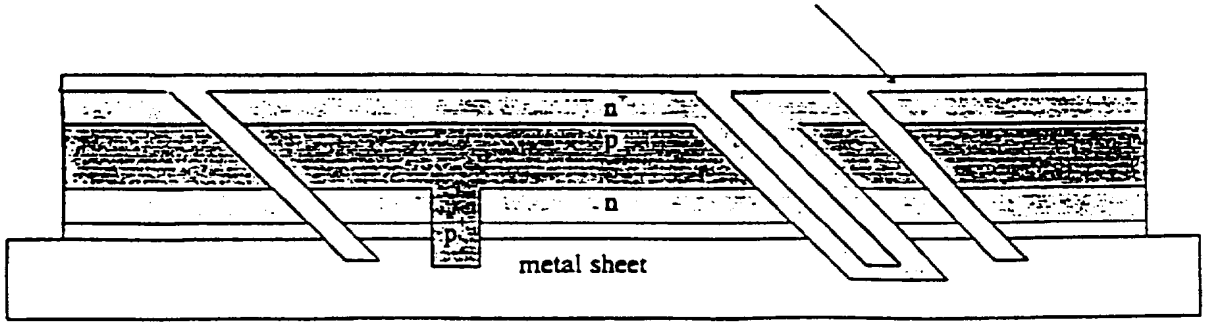


Fig 12

6. solid phase crystallisation of silicon layers (if necessary)

7. encapsulate, then scribe line in rear metal to isolate n from p contacts within individual cells:

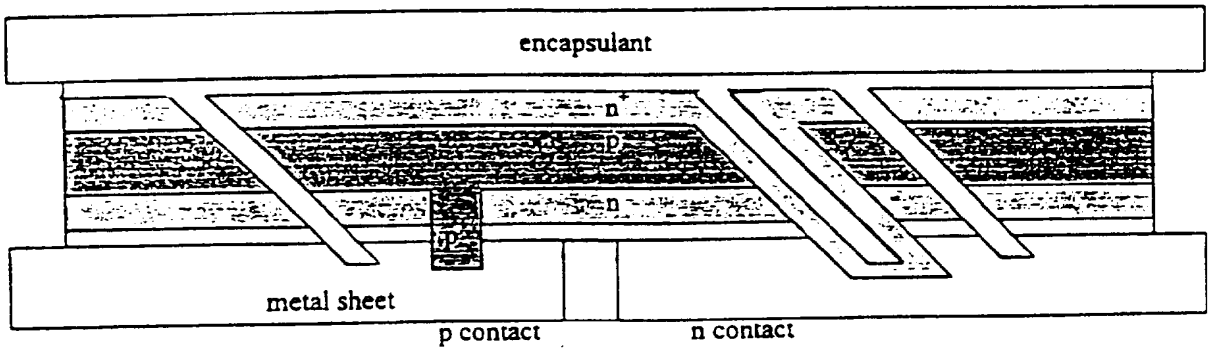


Fig 13

Rear Point Contacting Scheme (#2a) for a Glass Superstrate

1. deposit silicon layers and crystallise (initial passivating di-electric layer / AR coating not shown):

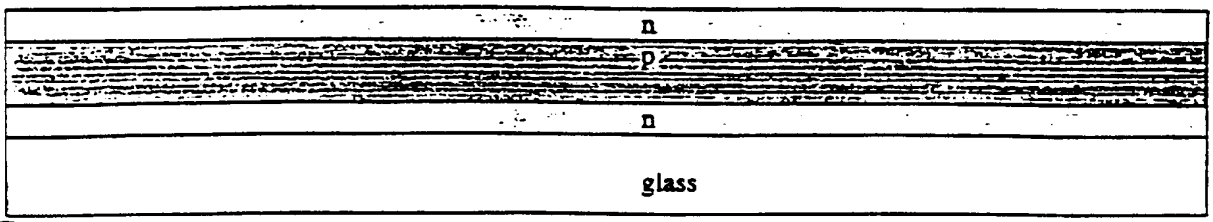
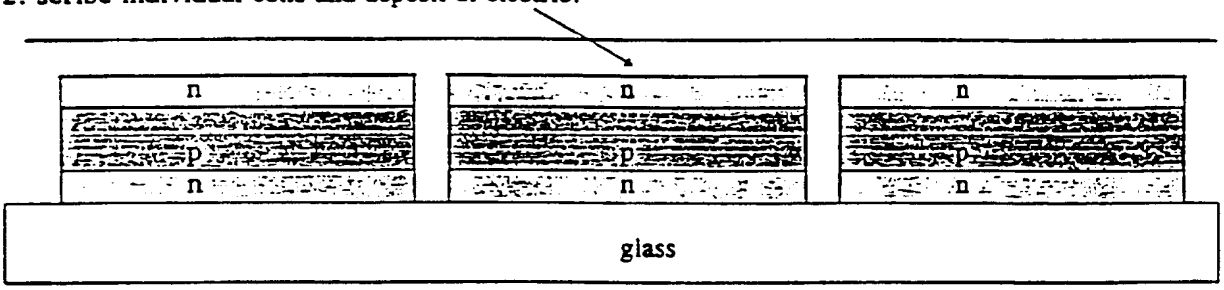


Fig 14

2. scribe individual cells and deposit di-electric:



(Note that for conventional cells, this step is reached simply by placing diffused, oxidised, un-contacted wafers on the glass.)

Fig 15

3. deposit metal:

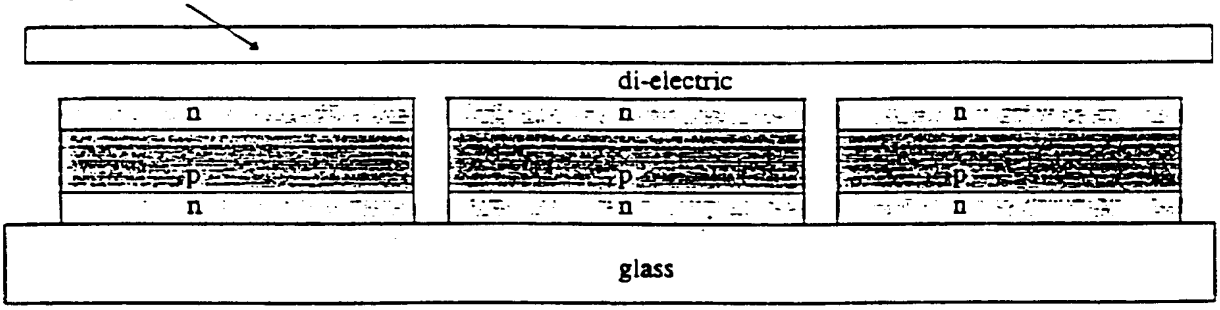


Fig 16

4. laser ablation of contact holes, followed by n^+ silicon deposition:

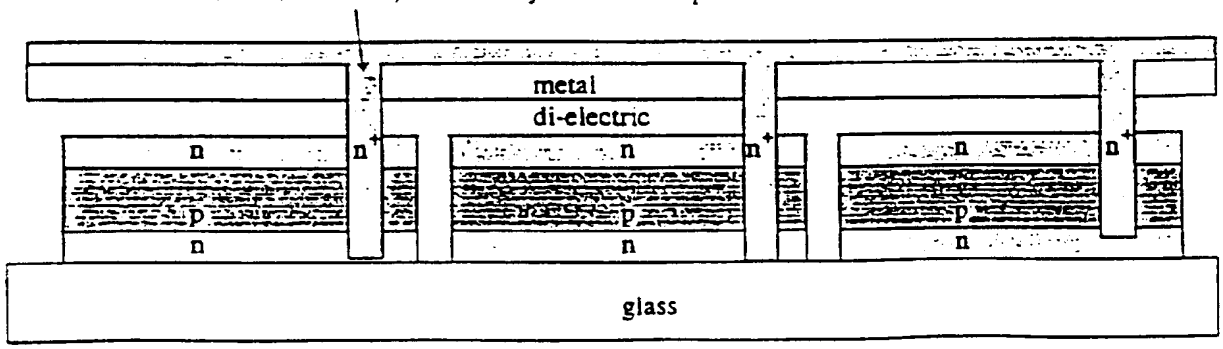
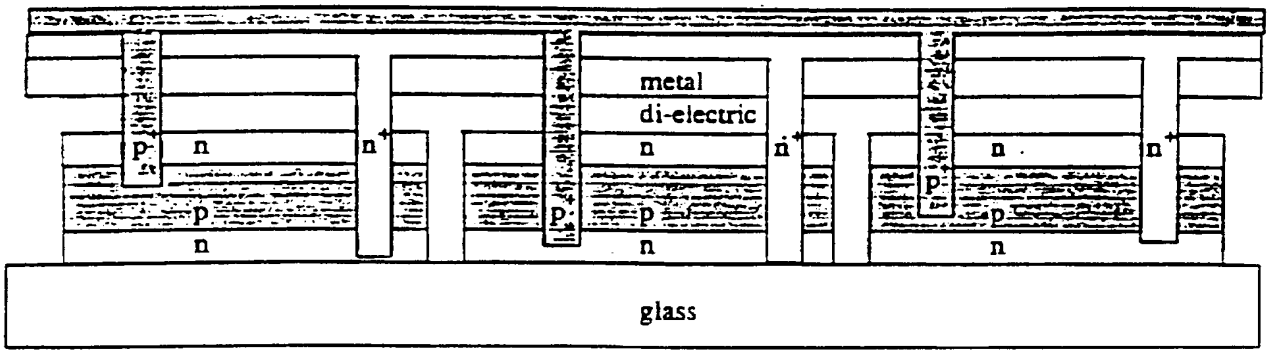


Fig 17

5. laser ablation of p^+ contact holes. followed by p^+ silicon deposition:



note p^+ silicon is connected to metal at the hole edges.

Fig 18

6. scribe lines to isolate n^+ from p^+ within individual cells :

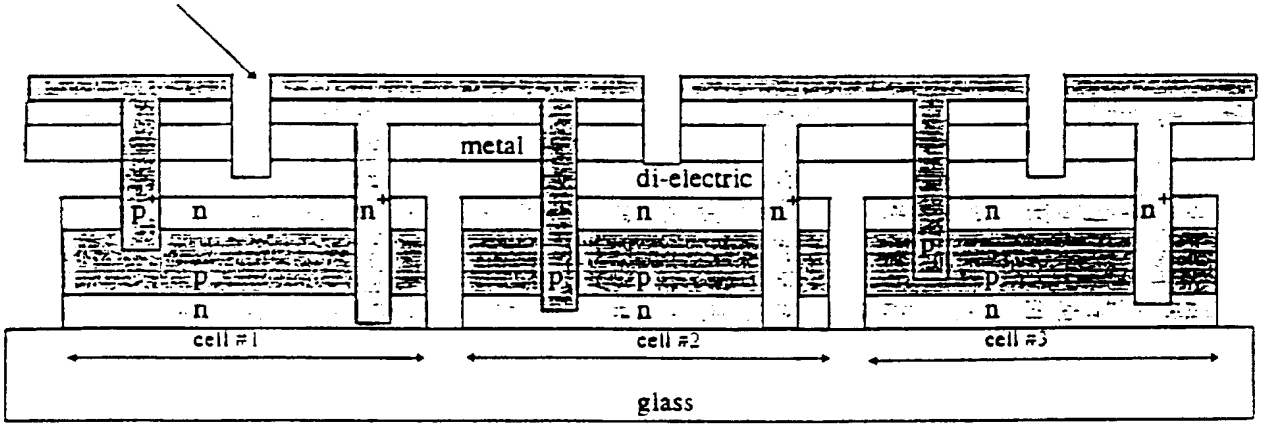


Fig 19

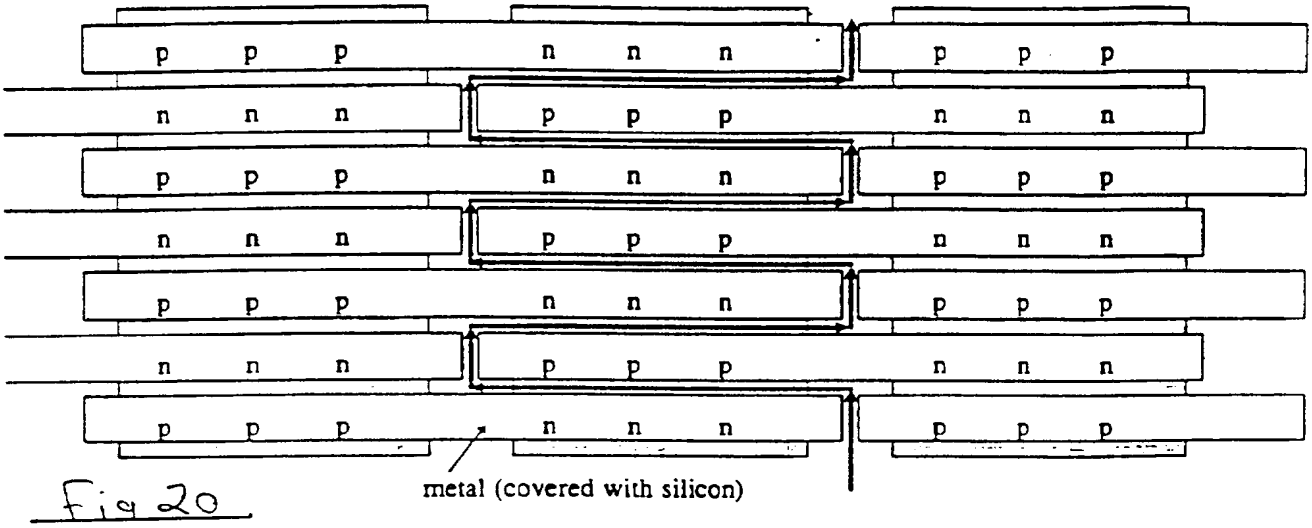


Fig 20

n and p are contact holes of the corresponding polarity

The same effect can be achieved using two sets of straight scribes:

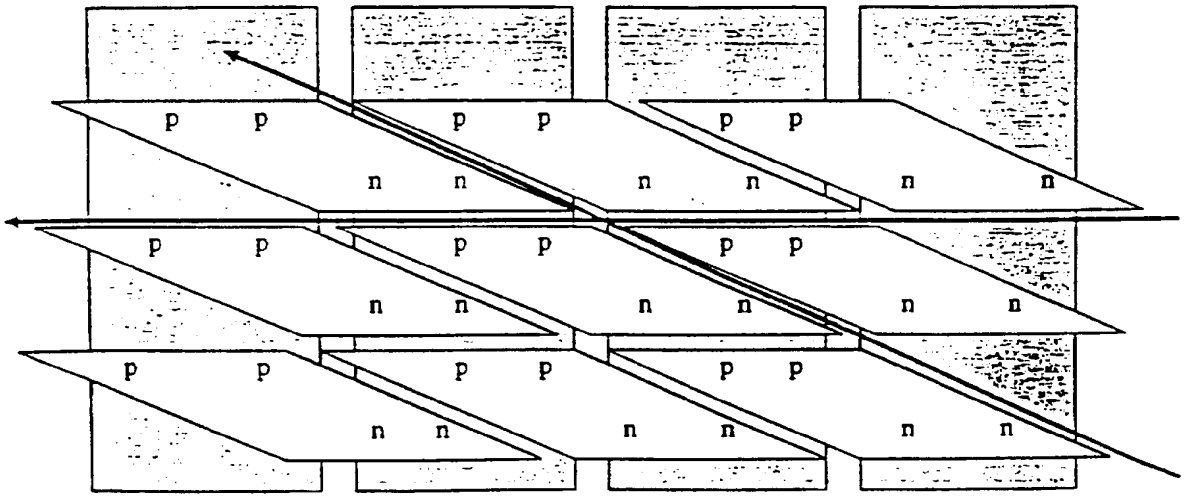


Fig 21

Alternative Rear Point Contacting Scheme (#2b) for a Metal Substrate

1. deposit di-electric layer and silicon layers:

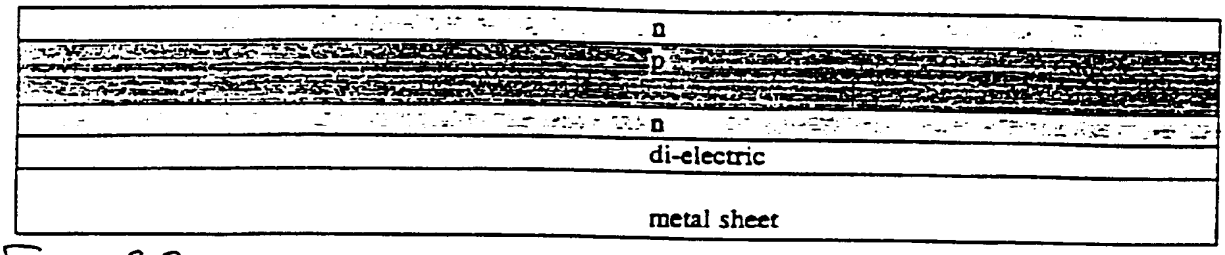


Fig 22

2. scribe isolated cells, deposit di-electric and (if necessary) crystallise silicon:

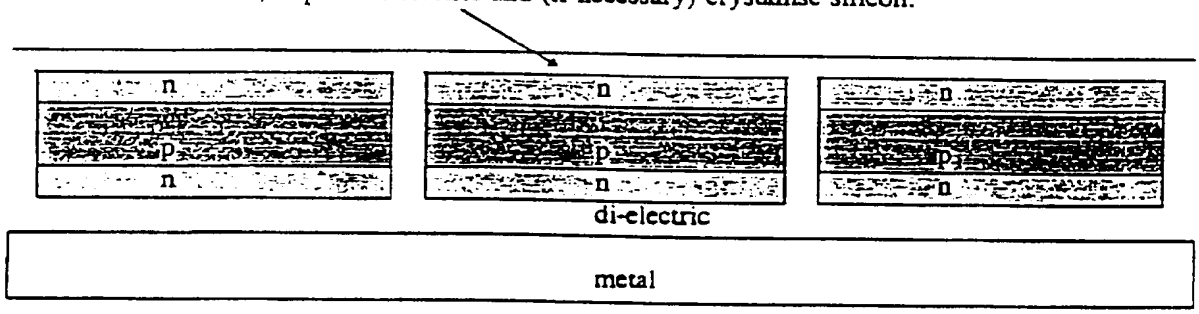


Fig 23

turn over substrate:

3. laser ablation of contact holes, followed by n^+ silicon deposition :

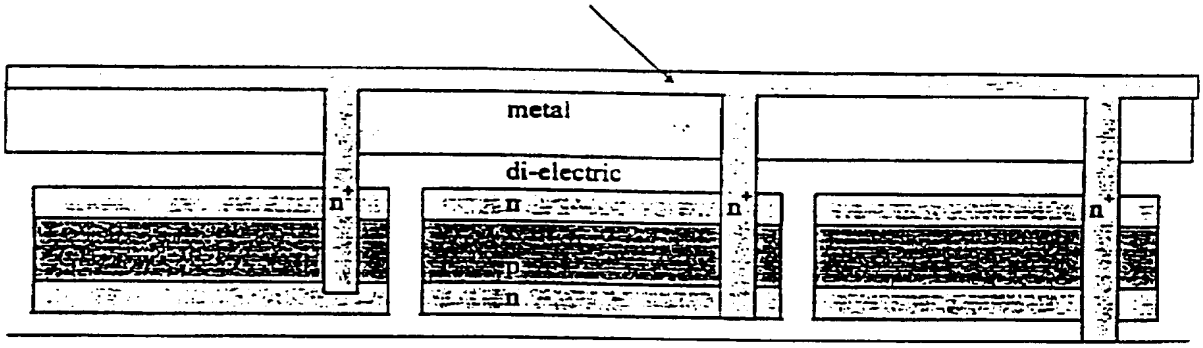


Fig 24

4. laser ablation of holes, followed by p^+ silicon deposition:

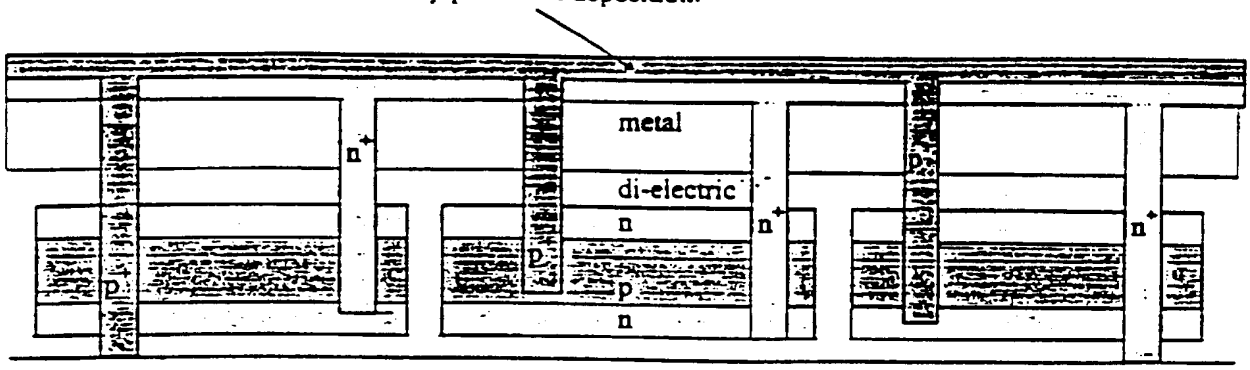
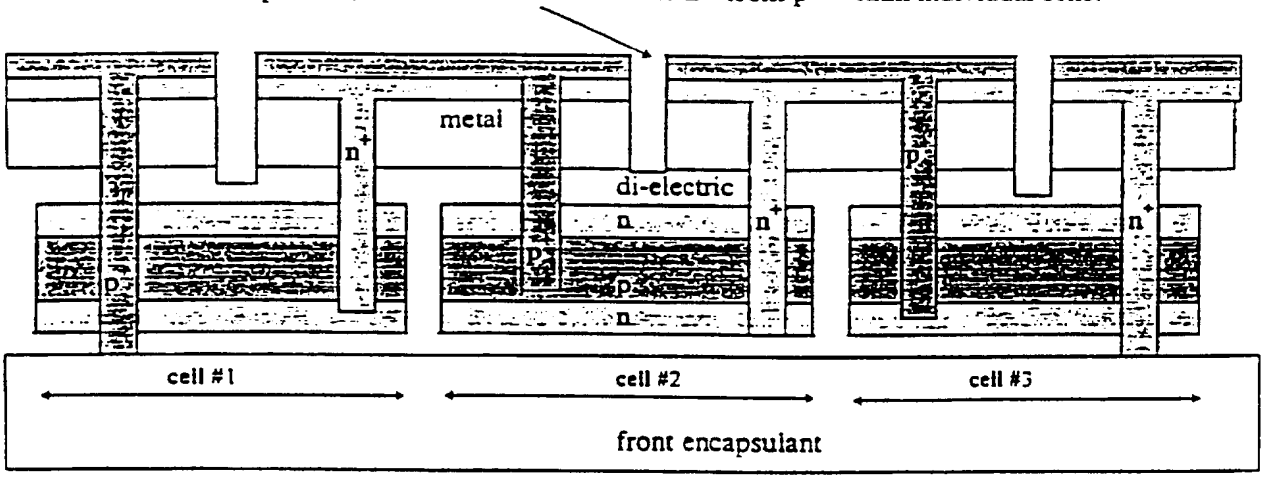


Fig 25

6. attach to front encapsulant, then scribe lines to isolate n^+ from p^+ within individual cells:



Note that the encapsulant is the supporting layer once the continuity of the metal substrate is broken.

The structure is now similar to scheme #2a for glass superstrates.

Fig 26

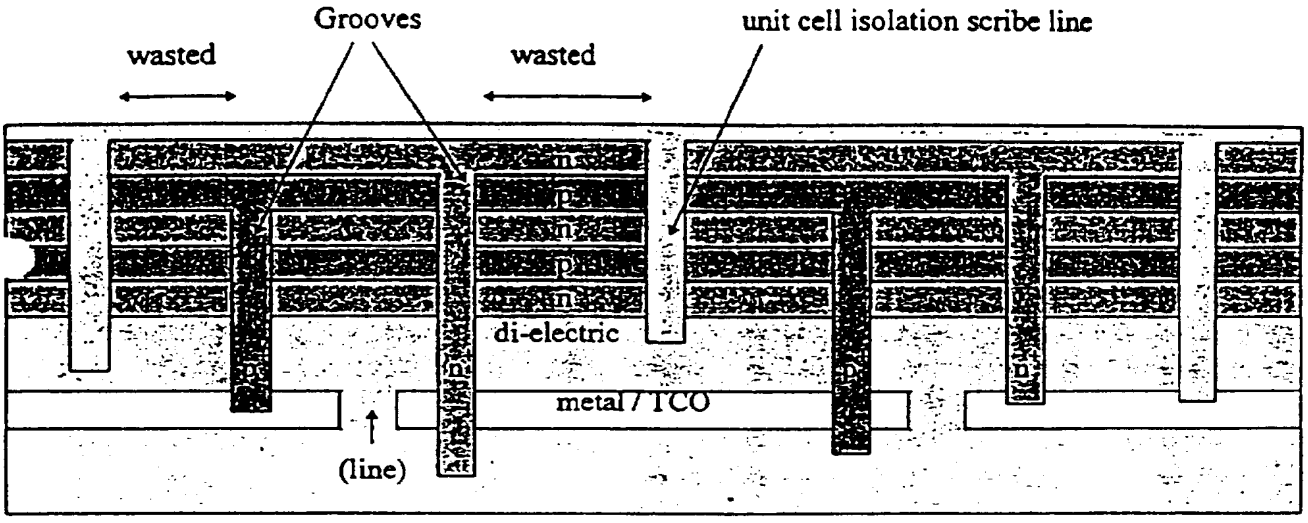

Grooves
unit cell isolation scribe line
wasted
wasted
di-electric
metal / TCO
(line)

Fig 27

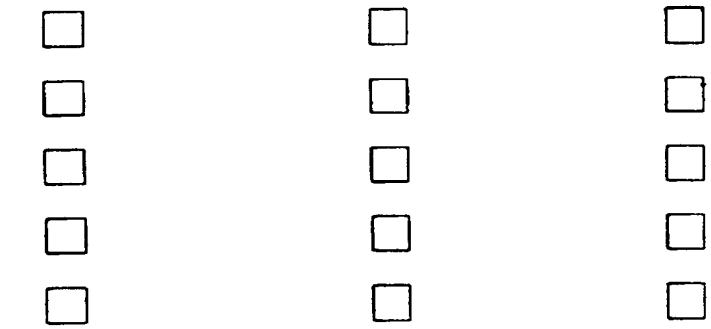
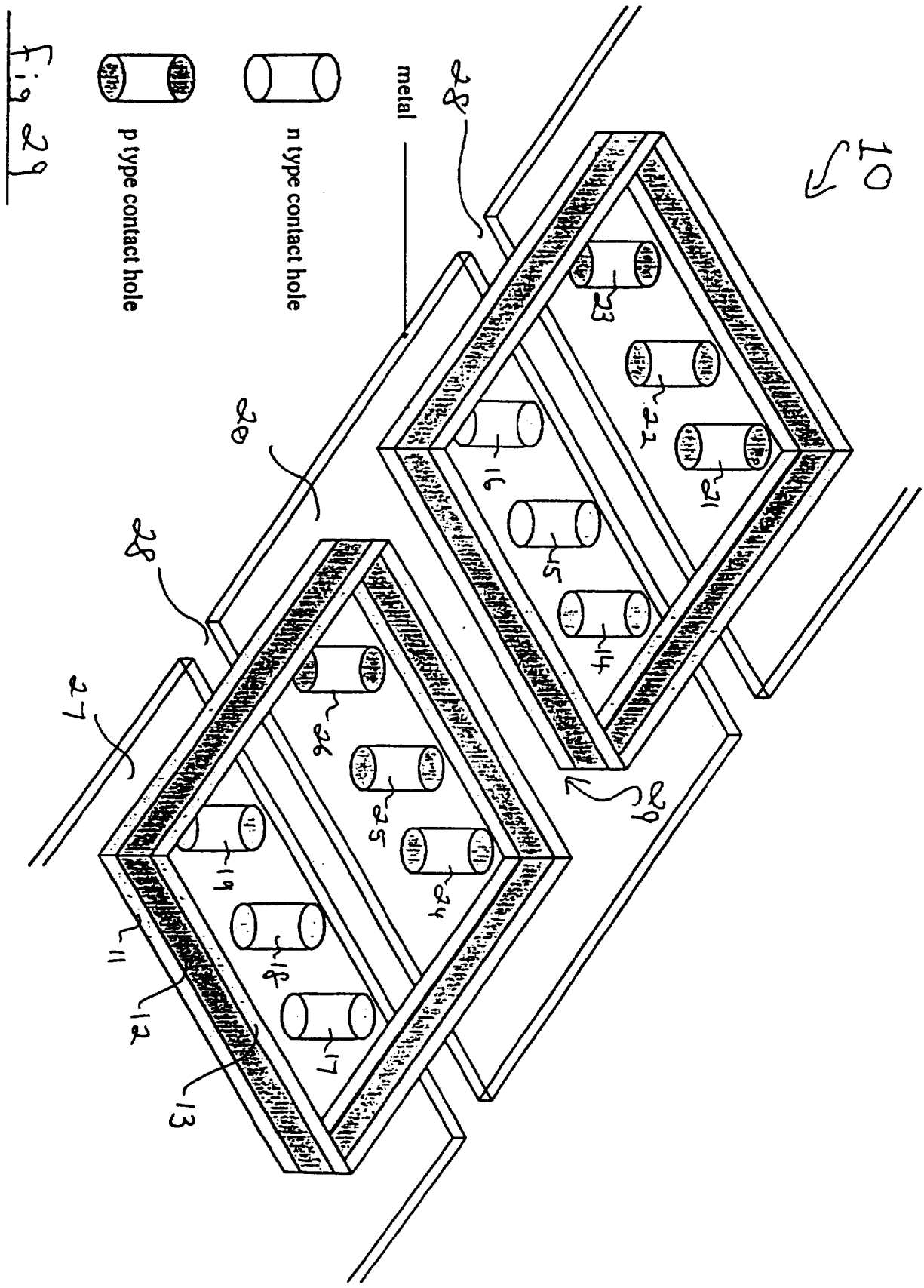


Fig 28


p type contact hole
n type contact hole
metal
10
11
12
13
14
15
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26
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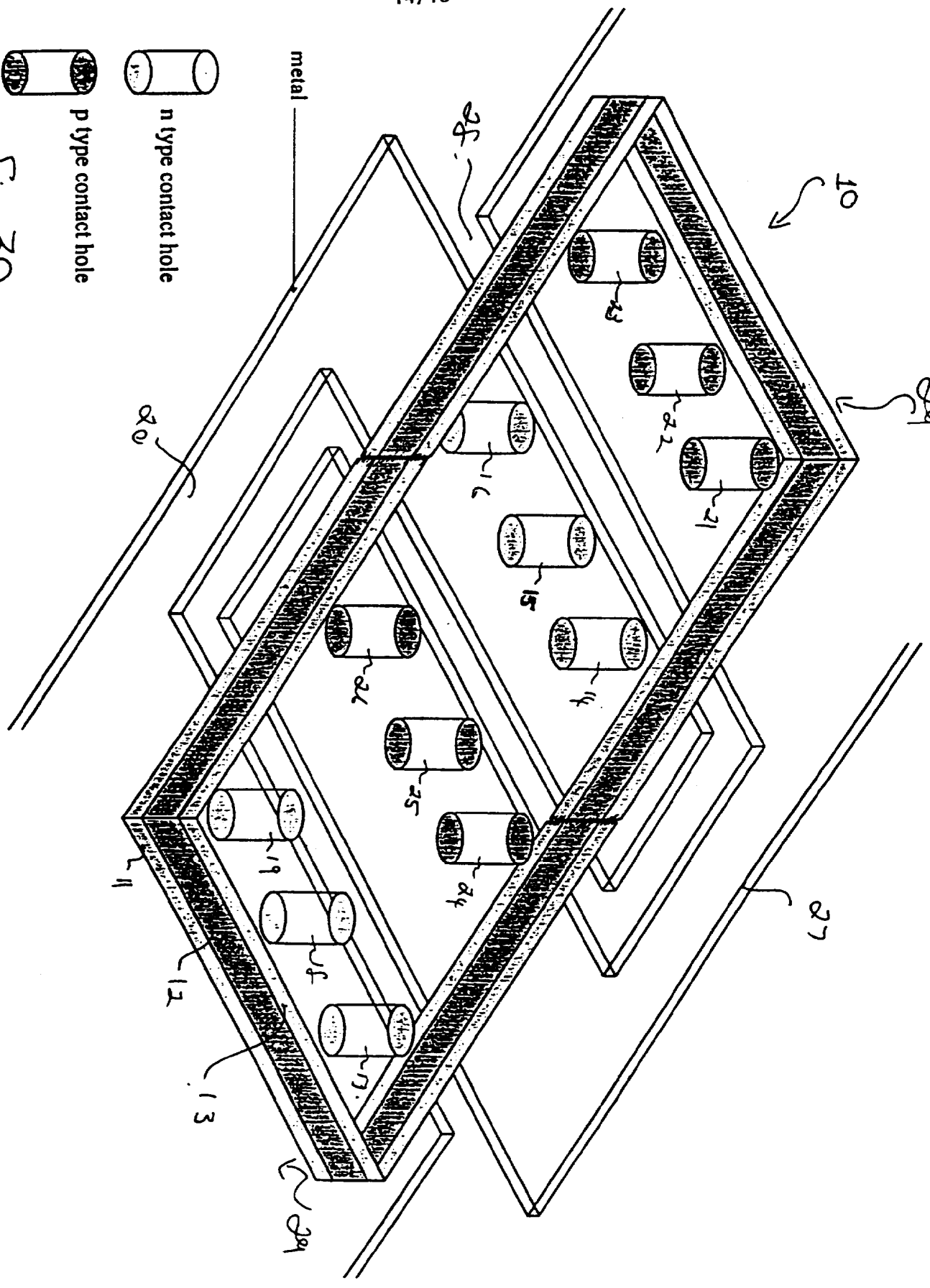
28

Fig 2a


p type contact hole
n type contact hole
metal
10
11
12
13
14
15
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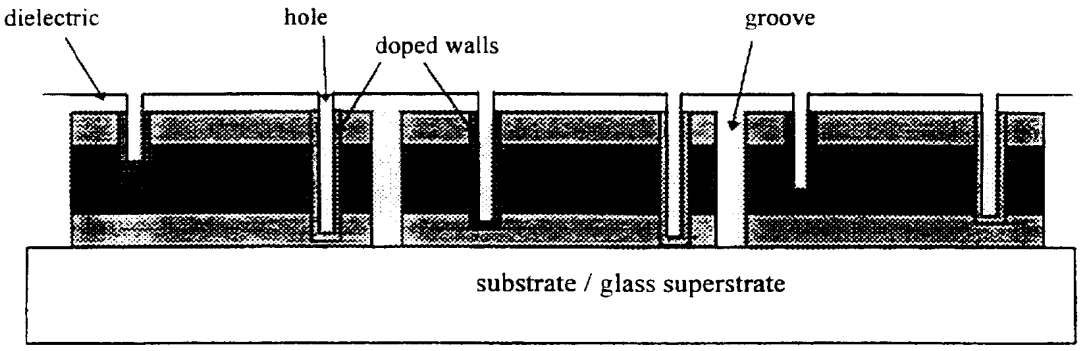
29

Fig 30

Contacting pipe walls to conducting plane using a conductor (rather than semiconductor)

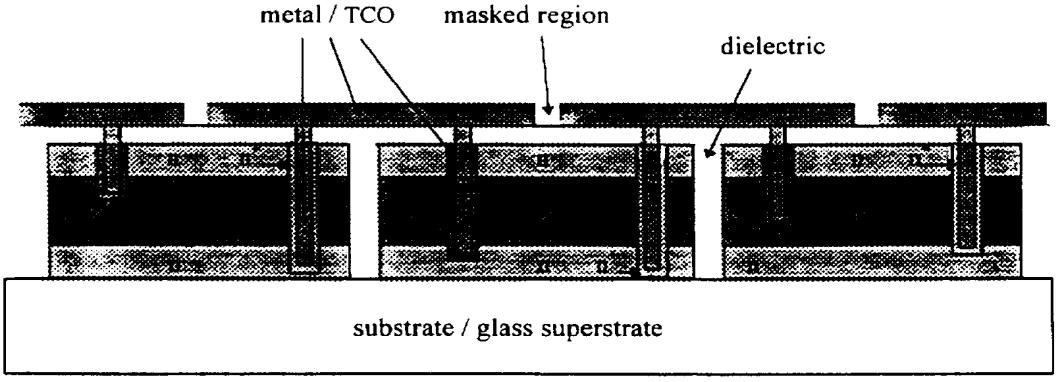
1. Deposit Si layers, groove into individual cells, coat with dielectric, then form holes and dope walls of holes:



Doping of hole walls could be performed by either:

- simultaneous laser ablation and doping
- form one set of holes and blanket deposit n-type dopant source (ie. into holes), then form second set of holes and perform diffusion in p-type dopant atmosphere (n-type dopant goes into first set of holes, p-type dopant goes into second set)

2. Deposit a conductor (eg. metal/TCO), by evaporation through a shadow mask, or by screen printing:



Compared to previous scheme for glass superstrates, extra silicon deposition steps and scribing of metal layer are avoided, but extra steps are required to dope the pipe walls.

Transparent Conducting Oxide (TCO) would be used for opaque substrates, or bifacial modules on glass sub/superstrates.

Fig 31

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 96/00793

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl[6]: H01L 31/05, 27/142, 31/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: H01L 31/05, 27/142, 31/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DERWENT, JAPIO: H01L 31/05, 27/142
H01L 31/18 with keywords (SOLAR) and (CONTACT: or INTERCONNECT: or GROOVE: or INTER()CONNECT:)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 93/12543 A (UNISEARCH LIMITED) 24 June 1993 whole document	1-13, 15-20
X	US 5468652 A (GEE) 21 November 1995 whole document	1-13, 15-20
X	US 4626613 A (WENHAM et al.) 2 December 1986 Claims 6-7; column 6, line 30 - column 7, line 5; figure 10	1-3

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 March 1997	9 APR 1997

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INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 96/00793

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5421908 A (YOSHIDA et al.) 6 June 1995 column 2, line 60 - column 5, line 32; figures 10a, 10b	1-3
X	EP 618623 A (SIEMENS AG) 5 October 1994 [& US 5494832 A (LEHMANN et al.) 27 February 1996] Abstract; figure 11	1-13
X	CA 2024662 A (OSWALD R) 9 March 1991 [& US 5593901 A (OSWALD et al.) 14 January 1997] Abstract; figure 2g	1-3
X	US 5391236 A (KRUT et al.) 21 February 1995 Abstract; figure 1g	1
A	EP 201312 A (ATLANTIC RICHFIELD COMPANY) 12 November 1986 Abstract; figure 2	

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 96/00793

Box 1 Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 14
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Claim 14 does not comply with Rule 6.2(a) of the PCT.

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No.
PCT/AU 96/00793

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	93/12543	AU	30781/92	EP	616727	JP	7-501660
		US	5595607				
US	5468652		NONE				
US	4626613	AU	36664/84	DE	3446885	JP	60-158678
		JP	8-037318				
US	5421908	DE	4344693	JP	6-342924		
EP	618623	DE	4310206	JP	6-302839	US	5494832
CA	2024662	CN	1050793	EP	427934	JP	3-171675
		US	5593901				
US	5391236		NONE				
EP	201312	US	4724011	DE	3686195	JP	61-260683

END OF ANNEX